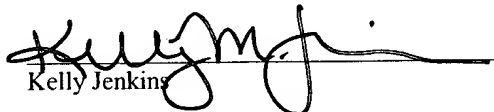


CERTIFICATE OF MAILING

I hereby certify that this correspondence (along with any paper referred to as being attached enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313 - 1450

Date: 10-14-03

  
Kelly Jenkins

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re patent application of:

Applicant(s): Bharath Rangarajan, *et al.*

Examiner: Richard A. Rosenberger

Serial No: 09/893,803

Art Unit: 2877

Filing Date: June 28, 2001

Title: SYSTEM AND METHOD FOR CREATION OF SEMICONDUCTOR MULTI-SLOPED FEATURES

**Mail Stop Appeal Brief-Patents  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450**

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APPEAL BRIEF

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Dear Sir:

Applicants' representative submits this brief in triplicate in connection with an appeal for the above-identified application. Please charge the requisite fee associated with this brief to Deposit Account No. 50-1063 (Reference Number AMDP660US).

10/22/2003 AUCNDATA 00000082 501063 09833803

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**I. Real Party in Interest (37 C.F.R. § 1.192(c)(1))**

The real party in interest in the present appeal is ADVANCED MICRO DEVICES the assignee of the present application.

**II. Related Appeals and Interferences (37 C.F.R. § 1.192(c)(2))**

Appellant, appellant's legal representatives, and/or the assignee of the present application are unaware of any appeals or interferences which will directly affect, or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**III. Status of Claims (37 C.F.R. § 1.192(c)(3))**

Claims 1-29 are pending in the application. The rejection of claims 1-29 is appealed. Claim 30 has been withdrawn from consideration by the Examiner.

**IV. Status of Amendments (37 C.F.R. § 1.192(c)(4))**

No amendments have been filed subsequent to final rejection.

**V. Summary of Invention (37 C.F.R. § 1.192(c)(5))**

Applicants' claimed invention relates to methods and systems for *regulating* an etch process, when creating multi-sloped elements on a wafer surface. Such a system continuously collects parameters that can indicate a progress of the associated etching process, and the manner sloped features on a wafer are being developed at a given time. Based on such parameters, the system can *in-situ* adjust the associated etching process to obtain desired sloped geometry on the wafer's surface.

The system collects the parameters required for etching a sloped feature, from the wafer's surface via a light reflection (*e.g. scatterometry*) technique. The wafer is illuminated via a light source (*e.g. frequency stabilized laser, laser diode, helium neon gas laser*), and light reflected from the wafer's surface is collected by one or more light receivers. (Specification at p.10, lines 20-30.) A measuring system, which can include a scatterometry component, interprets or converts the received light in to measured data. Such measured data, for example can be extracted by comparing properties of light (*e.g. phase, intensity*) *reflected* from the wafer surface with properties of light directed to the wafer surface, and correspond to parameters indicative of progression of the etch

process on the wafer's surface, *e.g.* thickness of created features, feature slope, and the like. (Specification at p.18, last paragraph continued into p.19.) A processor then compares such measured data with values stored in a *signature* data base, and accordingly adjusts the etch mechanism to fabricate the desired sloped features on the wafer's surface. (Specification at p.13, lines 14-22; *See also* p.19, last paragraph).

It is respectfully submitted that the cited art fails to teach or suggest these claimed features, as will be discussed in greater detail below.

**VI. Statement of the Issues (37 C.F.R. § 1.192(c)(6))**

Whether claims 1-29 are properly rejected under 35 U.S.C. §103(a) as being obvious over Ausschnitt (US Patent 5,629,772) in view of Coronel *et al.* (US Patent 5,658,418).

**VII. Grouping of Claims (37 C.F.R. § 1.192(c)(7))**

For the purposes of this appeal only, the claims are grouped as follows:

Claims 1, 8, 12-14 stand or fall together, and claims 2-7, 9-11, 15-29 stand or fall together.

**VIII. Argument (37 C.F.R. § 1.192(c)(8))**

**Rejection of Claims 1-29 Under 35 U.S.C. §103(a)**

Claims 1-29 stand rejected under 35 U.S.C. §103(a) as being obvious over Ausschnitt in view of Coronel *et al.* A reversal of the rejection is respectfully requested for at least the following reasons.

- i. The cited references, alone or in combination, fail to teach or suggest a system for measuring a parameter required for creating a sloped feature (e.g. angular detections), as the purported combination limits measurements to a feature's orthogonal distances.*

Applicants' claimed invention is directed to creating multi sloped features on a wafer surface. Neither Ausschnitt, alone or in combination with Coronel *et al.* teach or suggest a system for regulating an etch process for creating *multi-sloped features*, *e.g.* determining angular detections, by analyzing properties of light reflected from a wafer's surface, as in the subject claims.

Rather, Ausschnitt measures a difference in an actual "printed" feature's *length* in a pattern array of the resist image, from its "nominal" length, (*i.e.* measures a length "bias"), and calculates a

respective **width** bias associated with the printed feature. *See* Ausschnitt Fig. 1, *See also* col. 6, lines 48-65. Accordingly, Ausschnitt's measurements are limited to measuring a length and width projection of the features in a horizontal plane. Such is not measuring an etch parameter ***required to fabricate a multi-sloped feature*** being formed in space *via* properties of light reflected from a wafer's surface, *e.g.* intensity change, phase change, as in applicants' claimed invention.

In addition, Coronel *et al.* fails to make up for the aforementioned deficiencies of Ausschnitt with respect to the subject claims. Coronel *et al.* is directed to determining a vertical distance (thickness) from start to end of an etch process. Accordingly, the purported combination can only determine features in orthogonal distances (length, width and height) - not angles, slope inclinations or other etch parameters ***required to fabricate a multi-sloped feature*** as in applicants' claimed invention.

For at least the above reasons rejection of the subject claims is improper, and a reversal of this rejection is respectfully requested.

***ii. The Office Action rejects the subject claims even though it concedes that relied upon references fail to teach or suggest a scatterometry component that is part of the measuring device.***

Dependent claim 2 of the subject invention recites; "***scatterometry system [...] interprets the reflected light to produce the measured etch parameters***". Claims 3-7, 9-11, 15-29 recite similar limitations. Such a scatterometry technique provides for advantages over conventional systems, such as the cited art. In particular, etch parameters, such various angles, and spatial slope inclinations typically required for multi slope etch processing, can be measured via such scatterometry technique.

Ausschnitt, alone or in combination with Coronel *et al.* fails to teach or suggest a scatterometry component as part of the measuring system that measures an etch parameters *via* properties of reflected light. As explained *supra*, Ausschnitt calculates a width bias, *i.e.*, a difference between a feature's actual imprinted width and the nominal width *via* an equation that requires a measured length of the feature – no scatterometry technique as in applicants' claimed invention is taught or suggested by Ausschnitt. In addition, Coronel *et al.* fails to make up for the aforementioned deficiencies of Ausschnitt with respect to the subject claims. Coronel employs a "***spectro-meter***" that measures a layer's thickness by altering wave lengths – not a scatterometry

technique, which operates *via*, for example, a phase or intensity change of the reflected light, as recited in the subject claims.

Despite the lack of teaching of such inventive feature in the cited references, let alone even motivation to modify the references in the manner suggested, the Examiner rejects the subject claims. In general, the rationale proffered to combine the references and/or modify the references is to achieve benefits identified in applicants' specification, which overcome problems associated with conventional systems/methods. Applicants' representative respectfully submits that this is an unacceptable and improper basis for a rejection under 35 U.S.C. §103. In essence, the Examiner is basing the rejection on the assertion that it would have been obvious to do something not suggested in the art because so doing would provide advantages stated in applicants' specification. This type of rationale has been condemned by the CAFC. *See for example, Panduit Corp. v. Dennison Manufacturing Co.*, 1 USPQ2d 1593 (Fed. Cir. 1987)

Moreover, contrary to assertions made in the Office Action, the fact that scatterometry systems are well known in the art (as noted in the subject specification) does not make obvious use of a scatterometry system in connection with generation of multi-sloped profiles, as recited in the subject claims.


***...‘virtually all [inventions] are combinations of old elements.’*** Therefore an examiner may often find every element of a claimed invention in the prior art. ***If identification of each claimed element in the prior art were sufficient to negate patentability, very few patents would ever issue.*** Furthermore, rejecting patents solely by finding prior art corollaries for the claimed elements would permit an examiner to use the claimed invention itself as a blueprint for piecing together elements in the prior art to defeat the patentability of the claimed invention. ***Such an approach would be ‘an illogical and inappropriate process by which to determine patentability.’*** *In re Rouffet*, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453 (Fed. Cir. 1998) (*citations omitted*).

For at least the above reasons rejection of claims 2-7, 9-11, 15-29 is improper, and a reversal of this rejection is respectfully requested.

**IX. Conclusion**

For at least the above reasons, the claims currently under consideration are believed to be patentable over the cited references. Accordingly, it is respectfully requested that the rejections of claims 1-29 be reversed.

Respectfully submitted,  
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**X. Appendix of Claims (37 C.F.R. § 1.192(c)(9))**

1. (Original) A system for *in-situ* regulation of an etch process employed in fabricating a multi-sloped semiconductor feature on a wafer, comprising:

one or more etching components operative to etch at least one aspect of a multi-sloped feature on a wafer;

an etch component controller for controlling the one or more etching components;

a system for directing light onto the wafer;

a measuring system for measuring at least one etching parameter based on light reflected from the wafer; and

a process analyzer operatively coupled to the measuring system and the etch component controller, wherein the process analyzer receives the measured parameters from the measuring system and analyzes the measured parameters to determine whether adjustments to the etching components are needed to fabricate the multi-sloped features within desired critical dimension tolerances and where the process analyzer stores the measured parameters to facilitate reproducing process conditions.

2. (Original) The system of claim 1, the measuring system further including a scatterometry system for collecting the reflected light, wherein the measuring system interprets the reflected light to produce the measured etch parameters using scatterometry techniques.

3. (Original) The system of claim 2, wherein the measured etch parameters include at least one of feature height, feature width, slope of one or more feature sides and angles between feature sides.

4. (Original) The system of claim 3, wherein the multi-sloped feature has one or more angles between feature sides that are not right angles.

5. (Original) The system of claim 2, wherein the process analyzer:

partitions the wafer into a plurality of grid blocks; and

determines whether to make adjustments to one or more etching components associated with

one or more grid blocks by analyzing measured etch parameters corresponding to one or more grid blocks.

6. (Original) The system of claim 5, wherein the process analyzer determines that adjustments to one or more etching components are necessary for at least a portion of the wafer by comparing one or more measured etch parameter values to one or more stored acceptable etch parameter values.

7. (Original) The system of claim 6, wherein the stored acceptable etch parameter values are stored as scatterometry signatures.

8. (Original) A method for *in-situ* regulation of a process for etching a multi-sloped semiconductor device formed on a wafer, comprising:

- partitioning the wafer into one or more portions;
- etching at least one multi-sloped device on at least one portion of the wafer;
- directing light onto at least one portion of the wafer;
- collecting light reflected from the at least one portion;
- analyzing the reflected light to determine the acceptability of the multi-sloped semiconductor device on the at least one portion;
- storing data associated with the acceptability of the multi-sloped semiconductor device and one or more processing conditions associated with creating the multi-sloped semiconductor device to facilitate reproducing the one or more processing conditions; and
- selectively controlling one or more etching components to regulate the etching of the multi-sloped semiconductor device on the at least one portion.

9. (Original) The method of claim 8, wherein the light is collected by a scatterometry measuring system.

10. (Original) The method of claim 9, wherein the scatterometry measuring system interprets the reflected light into measured etch parameters associated with the at least one portion using scatterometry techniques.



11. (Original) The method of claim 10, wherein the measured etch parameters are compared to stored acceptable etch parameter values in order to determine whether one or more adjustments to the process for etching a multi-sloped semiconductor device formed on a wafer is necessary.

12. (Original) A method for *in-situ* regulation of an etch process of a multi-sloped semiconductor device formed on a wafer, comprising:

- partitioning the wafer into a plurality of grid blocks;
- using one or more etching components to etch a multi-sloped semiconductor feature on the wafer, each etching component functionally corresponding to a respective grid block;
- measuring at least one etch parameter associated with the multi-sloped semiconductor feature;
- determining etching conditions at the at least one grid block according to the measured etch parameter; and
- using a process analyzer to selectively control the plurality of etching components to compensate for wafer to wafer variations during the etch process of the multi-sloped feature.

13. (Original) A system for *in-situ* regulation of an etch process of a multi-sloped semiconductor device formed on a wafer, comprising:

- means for partitioning the wafer into a plurality of portions;
- means for etching at least one multi-sloped device on at least one portion of the wafer;
- means for directing light onto at least one portion of the wafer;
- means for collecting light reflected from the at least one portion;
- means for analyzing the reflected light to determine the acceptability of the etching of the at least one portion; and
- means for selectively controlling one or more etching components to regulate the etching of the multi-sloped semiconductor device on the at least one portion.

14. (Original) A data packet adapted to be transmitted between two or more processes, the data packet containing information related to *in-situ* adaptation of an etch process employed in fabricating a multi-sloped semiconductor device, where the information was generated by a system

for *in-situ* regulation of an etch process employed in fabricating a multi-sloped semiconductor feature on a wafer, the system comprising:

- one or more etching components operative to etch at least one aspect of a multi-sloped feature on a wafer;

- an etch component controller for controlling the one or more etching components;

- a system for directing light onto the wafer;

- a measuring system for measuring at least one etching parameter based on light reflected from the wafer; and

- a process analyzer operatively coupled to the measuring system and the etch component controller, wherein the process analyzer receives the measured parameters from the measuring system and analyzes the measured parameters to determine whether adjustments to the etching components are needed to fabricate the multi-sloped features within desired critical dimension tolerances and where the process analyzer stores the measured parameters to facilitate reproducing process conditions.

15. (Previously Added) A method employed for manufacturing semiconductor devices, comprising:

- determining a desired multi-sloped profile;

- etching at least one device to conform to the desired multi-sloped profile;

- detecting *in situ* parameters of the etching of the device utilizing scatterometry;

and

- adjusting the etching of the multi-sloped profile as necessary to produce the desired multi-sloped profile.

16. (Previously Added) The method of claim 15, further including storing the desired multi-sloped profile.

17. (Previously Added) The method of claim 15, further including analyzing the parameters of the etching of the device.

18. (Previously Added) The method of claim 17, wherein analyzing includes comparing current parameters to previous parameters.

19. (Previously Added) The method of claim 15, further including storing the parameters found while detecting *in situ* parameters.

20. (Previously Added) The method of claim 15, wherein adjusting the etching of the multi-sloped profile includes at least one from a group consisting of reducing a rate of etching and increasing a rate of etching.

21. (Previously Added) The method of claim 15, further including controlling light sources utilized in detecting *in situ* parameters.

22. (Previously Added) The method of claim 21, wherein controlling light sources includes at least one from a group consisting of reducing a light source intensity, increasing a light source intensity and altering an angle of a light source.

23. (Previously Added) The method of claim 15, further including controlling light receivers utilized in detecting *in situ* parameters.

24. (Previously Added) The method of claim 23, wherein controlling light receivers includes at least one from a group consisting of reducing a light receiver sensitivity, increasing a light receiver sensitivity and altering an angle of a light receiver.

25. (Previously Added) A semiconductor device manufacturing system, comprising:  
at least one etch component for etching a device to conform to a desired multi-sloped profile;  
a detecting system employing scatterometry for detecting *in situ* parameters related to the etching of the device; and  
an etch component controller capable of receiving information from the detecting system to control the etch component as necessary to produce the desired multi-sloped profile.

26. (Previously Added) The system of claim 25, further comprising an analysis system to analyze *in situ* parameters provided by the detecting system.

27. (Previously Added) The system of claim 26, the analysis system additionally analyzes *in situ* parameters based on at least one from a group consisting of current *in situ* parameters, previous *in situ* parameters, scatterometry signature profiles, and predetermined multi-sloped profiles.

28. (Previously Added) The system of claim 25, further comprising a storage medium for storing at least one from a group consisting of current *in situ* parameters, previous *in situ* parameters, scatterometry signature profiles, and predetermined multi-sloped profiles.

29. (Previously Added) A system for manufacturing semiconductor devices, comprising:  
means for etching at least one device to conform to a desired multi-sloped profile;  
means for detecting *in situ* parameters of the etching of the device utilizing scatterometry; and  
means for adjusting the etching of the multi-sloped profile as necessary to produce the desired multi-sloped profile.

30. (Withdrawn)

PATENT

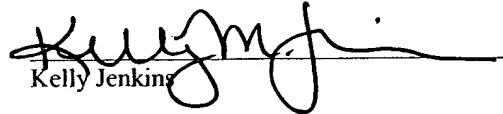
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Date: 10-14-03

  
Kelly Jenkins

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re patent application of:

Applicant(s): Bharath Rangarajan, *et al.*

Examiner: Richard A. Rosenberger

Serial No: 09/893,803

Art Unit: 2877

Filing Date: June 28, 2001

Title: SYSTEM AND METHOD FOR CREATION OF SEMICONDUCTOR MULTI-SLOPED FEATURES

**Mail Stop Appeal Brief-Patents  
Commissioner for Patents  
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APPEAL BRIEF

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Dear Sir:

Applicants' representative submits this brief in triplicate in connection with an appeal for the above-identified application. Please charge the requisite fee associated with this brief to Deposit Account No. 50-1063 (Reference Number AMDP660US).

**I. Real Party in Interest (37 C.F.R. § 1.192(c)(1))**

The real party in interest in the present appeal is ADVANCED MICRO DEVICES the assignee of the present application.

**II. Related Appeals and Interferences (37 C.F.R. § 1.192(c)(2))**

Appellant, appellant's legal representatives, and/or the assignee of the present application are unaware of any appeals or interferences which will directly affect, or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**III. Status of Claims (37 C.F.R. § 1.192(c)(3))**

Claims 1-29 are pending in the application. The rejection of claims 1-29 is appealed. Claim 30 has been withdrawn from consideration by the Examiner.

**IV. Status of Amendments (37 C.F.R. § 1.192(c)(4))**

No amendments have been filed subsequent to final rejection.

**V. Summary of Invention (37 C.F.R. § 1.192(c)(5))**

Applicants' claimed invention relates to methods and systems for *regulating* an etch process, when creating multi-sloped elements on a wafer surface. Such a system continuously collects parameters that can indicate a progress of the associated etching process, and the manner sloped features on a wafer are being developed at a given time. Based on such parameters, the system can *in-situ* adjust the associated etching process to obtain desired sloped geometry on the wafer's surface.

The system collects the parameters required for etching a sloped feature, from the wafer's surface via a light reflection (*e.g. scatterometry*) technique. The wafer is illuminated via a light source (*e.g. frequency stabilized laser, laser diode, helium neon gas laser*), and light reflected from the wafer's surface is collected by one or more light receivers. (Specification at p.10, lines 20-30.) A measuring system, which can include a scatterometry component, interprets or converts the received light in to measured data. Such measured data, for example can be extracted by comparing properties of light (*e.g. phase, intensity*) *reflected* from the wafer surface with properties of light directed to the wafer surface, and correspond to parameters indicative of progression of the etch

process on the wafer's surface, *e.g.* thickness of created features, feature slope, and the like. (Specification at p.18, last paragraph continued into p.19.) A processor then compares such measured data with values stored in a *signature* data base, and accordingly adjusts the etch mechanism to fabricate the desired sloped features on the wafer's surface. (Specification at p.13, lines 14-22; *See also* p.19, last paragraph).

It is respectfully submitted that the cited art fails to teach or suggest these claimed features, as will be discussed in greater detail below.

**VI. Statement of the Issues (37 C.F.R. § 1.192(c)(6))**

Whether claims 1-29 are properly rejected under 35 U.S.C. §103(a) as being obvious over Ausschnitt (US Patent 5,629,772) in view of Coronel *et al.* (US Patent 5,658,418).

**VII. Grouping of Claims (37 C.F.R. § 1.192(c)(7))**

For the purposes of this appeal only, the claims are grouped as follows:

Claims 1, 8, 12-14 stand or fall together, and claims 2-7, 9-11, 15-29 stand or fall together.

**VIII. Argument (37 C.F.R. § 1.192(c)(8))**

**Rejection of Claims 1-29 Under 35 U.S.C. §103(a)**

Claims 1-29 stand rejected under 35 U.S.C. §103(a) as being obvious over Ausschnitt in view of Coronel *et al.* A reversal of the rejection is respectfully requested for at least the following reasons.

- i. The cited references, alone or in combination, fail to teach or suggest a system for measuring a parameter required for creating a sloped feature (e.g. angular detections), as the purported combination limits measurements to a feature's orthogonal distances.*

Applicants' claimed invention is directed to creating multi sloped features on a wafer surface. Neither Ausschnitt, alone or in combination with Coronel *et al.* teach or suggest a system for regulating an etch process for creating *multi-sloped features*, *e.g.* determining angular detections, by analyzing properties of light reflected from a wafer's surface, as in the subject claims.

Rather, Ausschnitt measures a difference in an actual "printed" feature's *length* in a pattern array of the resist image, from its "nominal" length, (*i.e.* measures a length "bias"), and calculates a

respective **width** bias associated with the printed feature. *See* Ausschnitt Fig. 1, *See also* col. 6, lines 48-65. Accordingly, Ausschnitt's measurements are limited to measuring a length and width projection of the features in a horizontal plane. Such is not measuring an etch parameter ***required to fabricate a multi-sloped feature*** being formed in space *via* properties of light reflected from a wafer's surface, *e.g.* intensity change, phase change, as in applicants' claimed invention.

In addition, Coronel *et al.* fails to make up for the aforementioned deficiencies of Ausschnitt with respect to the subject claims. Coronel *et al.* is directed to determining a vertical distance (thickness) from start to end of an etch process. Accordingly, the purported combination can only determine features in orthogonal distances (length, width and height) - not angles, slope inclinations or other etch parameters ***required to fabricate a multi-sloped feature*** as in applicants' claimed invention.

For at least the above reasons rejection of the subject claims is improper, and a reversal of this rejection is respectfully requested.

ii. ***The Office Action rejects the subject claims even though it concedes that relied upon references fail to teach or suggest a scatterometry component that is part of the measuring device.***

Dependent claim 2 of the subject invention recites; "***scatterometry system [...] interprets the reflected light to produce the measured etch parameters***". Claims 3-7, 9-11, 15-29 recite similar limitations. Such a scatterometry technique provides for advantages over conventional systems, such as the cited art. In particular, etch parameters, such various angles, and spatial slope inclinations typically required for multi slope etch processing, can be measured via such scatterometry technique.

Ausschnitt, alone or in combination with Coronel *et al.* fails to teach or suggest a scatterometry component as part of the measuring system that measures an etch parameters *via* properties of reflected light. As explained *supra*, Ausschnitt calculates a width bias, *i.e.*, a difference between a feature's actual imprinted width and the nominal width *via* an equation that requires a measured length of the feature – no scatterometry technique as in applicants' claimed invention is taught or suggested by Ausschnitt. In addition, Coronel *et al.* fails to make up for the aforementioned deficiencies of Ausschnitt with respect to the subject claims. Coronel employs a "***spectro-meter***" that measures a layer's thickness by altering wave lengths – not a scatterometry



technique, which operates *via*, for example, a phase or intensity change of the reflected light, as recited in the subject claims.

Despite the lack of teaching of such inventive feature in the cited references, let alone even motivation to modify the references in the manner suggested, the Examiner rejects the subject claims. In general, the rationale proffered to combine the references and/or modify the references is to achieve benefits identified in applicants' specification, which overcome problems associated with conventional systems/methods. Applicants' representative respectfully submits that this is an unacceptable and improper basis for a rejection under 35 U.S.C. §103. In essence, the Examiner is basing the rejection on the assertion that it would have been obvious to do something not suggested in the art because so doing would provide advantages stated in applicants' specification. This type of rationale has been condemned by the CAFC. *See for example, Panduit Corp. v. Dennison Manufacturing Co.*, 1 USPQ2d 1593 (Fed. Cir. 1987)

Moreover, contrary to assertions made in the Office Action, the fact that scatterometry systems are well known in the art (as noted in the subject specification) does not make obvious use of a scatterometry system in connection with generation of multi-sloped profiles, as recited in the subject claims.

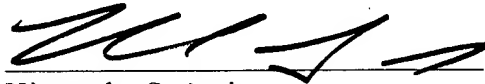
**...‘virtually all [inventions] are combinations of old elements.’** Therefore an examiner may often find every element of a claimed invention in the prior art. ***If identification of each claimed element in the prior art were sufficient to negate patentability, very few patents would ever issue.*** Furthermore, rejecting patents solely by finding prior art corollaries for the claimed elements would permit an examiner to use the claimed invention itself as a blueprint for piecing together elements in the prior art to defeat the patentability of the claimed invention. ***Such an approach would be ‘an illogical and inappropriate process by which to determine patentability.’*** *In re Rouffet*, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453 (Fed. Cir. 1998) (*citations omitted*).

For at least the above reasons rejection of claims 2-7, 9-11, 15-29 is improper, and a reversal of this rejection is respectfully requested.

**IX. Conclusion**

For at least the above reasons, the claims currently under consideration are believed to be patentable over the cited references. Accordingly, it is respectfully requested that the rejections of claims 1-29 be reversed.

Respectfully submitted,  
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**X. Appendix of Claims (37 C.F.R. § 1.192(c)(9))**

1. (Original) A system for *in-situ* regulation of an etch process employed in fabricating a multi-sloped semiconductor feature on a wafer, comprising:

one or more etching components operative to etch at least one aspect of a multi-sloped feature on a wafer;

an etch component controller for controlling the one or more etching components;

a system for directing light onto the wafer;

a measuring system for measuring at least one etching parameter based on light reflected from the wafer; and

a process analyzer operatively coupled to the measuring system and the etch component controller, wherein the process analyzer receives the measured parameters from the measuring system and analyzes the measured parameters to determine whether adjustments to the etching components are needed to fabricate the multi-sloped features within desired critical dimension tolerances and where the process analyzer stores the measured parameters to facilitate reproducing process conditions.

2. (Original) The system of claim 1, the measuring system further including a scatterometry system for collecting the reflected light, wherein the measuring system interprets the reflected light to produce the measured etch parameters using scatterometry techniques.

3. (Original) The system of claim 2, wherein the measured etch parameters include at least one of feature height, feature width, slope of one or more feature sides and angles between feature sides.

4. (Original) The system of claim 3, wherein the multi-sloped feature has one or more angles between feature sides that are not right angles.

5. (Original) The system of claim 2, wherein the process analyzer:  
partitions the wafer into a plurality of grid blocks; and  
determines whether to make adjustments to one or more etching components associated with

one or more grid blocks by analyzing measured etch parameters corresponding to one or more grid blocks.

6. (Original) The system of claim 5, wherein the process analyzer determines that adjustments to one or more etching components are necessary for at least a portion of the wafer by comparing one or more measured etch parameter values to one or more stored acceptable etch parameter values.

7. (Original) The system of claim 6, wherein the stored acceptable etch parameter values are stored as scatterometry signatures.

8. (Original) A method for *in-situ* regulation of a process for etching a multi-sloped semiconductor device formed on a wafer, comprising:

- partitioning the wafer into one or more portions;
- etching at least one multi-sloped device on at least one portion of the wafer;
- directing light onto at least one portion of the wafer;
- collecting light reflected from the at least one portion;
- analyzing the reflected light to determine the acceptability of the multi-sloped semiconductor device on the at least one portion;
- storing data associated with the acceptability of the multi-sloped semiconductor device and one or more processing conditions associated with creating the multi-sloped semiconductor device to facilitate reproducing the one or more processing conditions; and
- selectively controlling one or more etching components to regulate the etching of the multi-sloped semiconductor device on the at least one portion.

9. (Original) The method of claim 8, wherein the light is collected by a scatterometry measuring system.

10. (Original) The method of claim 9, wherein the scatterometry measuring system interprets the reflected light into measured etch parameters associated with the at least one portion using scatterometry techniques.

11. (Original) The method of claim 10, wherein the measured etch parameters are compared to stored acceptable etch parameter values in order to determine whether one or more adjustments to the process for etching a multi-sloped semiconductor device formed on a wafer is necessary.

12. (Original) A method for *in-situ* regulation of an etch process of a multi-sloped semiconductor device formed on a wafer, comprising:

- partitioning the wafer into a plurality of grid blocks;
- using one or more etching components to etch a multi-sloped semiconductor feature on the wafer, each etching component functionally corresponding to a respective grid block;
- measuring at least one etch parameter associated with the multi-sloped semiconductor feature;
- determining etching conditions at the at least one grid block according to the measured etch parameter; and
- using a process analyzer to selectively control the plurality of etching components to compensate for wafer to wafer variations during the etch process of the multi-sloped feature.

13. (Original) A system for *in-situ* regulation of an etch process of a multi-sloped semiconductor device formed on a wafer, comprising:

- means for partitioning the wafer into a plurality of portions;
- means for etching at least one multi-sloped device on at least one portion of the wafer;
- means for directing light onto at least one portion of the wafer;
- means for collecting light reflected from the at least one portion;
- means for analyzing the reflected light to determine the acceptability of the etching of the at least one portion; and
- means for selectively controlling one or more etching components to regulate the etching of the multi-sloped semiconductor device on the at least one portion.

14. (Original) A data packet adapted to be transmitted between two or more processes, the data packet containing information related to *in-situ* adaptation of an etch process employed in fabricating a multi-sloped semiconductor device, where the information was generated by a system

for *in-situ* regulation of an etch process employed in fabricating a multi-sloped semiconductor feature on a wafer, the system comprising:

one or more etching components operative to etch at least one aspect of a multi-sloped feature on a wafer;

an etch component controller for controlling the one or more etching components;

a system for directing light onto the wafer;

a measuring system for measuring at least one etching parameter based on light reflected from the wafer; and

a process analyzer operatively coupled to the measuring system and the etch component controller, wherein the process analyzer receives the measured parameters from the measuring system and analyzes the measured parameters to determine whether adjustments to the etching components are needed to fabricate the multi-sloped features within desired critical dimension tolerances and where the process analyzer stores the measured parameters to facilitate reproducing process conditions.

15. (Previously Added) A method employed for manufacturing semiconductor devices, comprising:

determining a desired multi-sloped profile;

etching at least one device to conform to the desired multi-sloped profile;

detecting *in situ* parameters of the etching of the device utilizing scatterometry;

and

adjusting the etching of the multi-sloped profile as necessary to produce the desired multi-sloped profile.

16. (Previously Added) The method of claim 15, further including storing the desired multi-sloped profile.

17. (Previously Added) The method of claim 15, further including analyzing the parameters of the etching of the device.

18. (Previously Added) The method of claim 17, wherein analyzing includes comparing current parameters to previous parameters.

19. (Previously Added) The method of claim 15, further including storing the parameters found while detecting *in situ* parameters.

20. (Previously Added) The method of claim 15, wherein adjusting the etching of the multi-sloped profile includes at least one from a group consisting of reducing a rate of etching and increasing a rate of etching.

21. (Previously Added) The method of claim 15, further including controlling light sources utilized in detecting *in situ* parameters.

22. (Previously Added) The method of claim 21, wherein controlling light sources includes at least one from a group consisting of reducing a light source intensity, increasing a light source intensity and altering an angle of a light source.

23. (Previously Added) The method of claim 15, further including controlling light receivers utilized in detecting *in situ* parameters.

24. (Previously Added) The method of claim 23, wherein controlling light receivers includes at least one from a group consisting of reducing a light receiver sensitivity, increasing a light receiver sensitivity and altering an angle of a light receiver.

25. (Previously Added) A semiconductor device manufacturing system, comprising:  
at least one etch component for etching a device to conform to a desired multi-sloped profile;  
a detecting system employing scatterometry for detecting *in situ* parameters related to the etching of the device; and

an etch component controller capable of receiving information from the detecting system to control the etch component as necessary to produce the desired multi-sloped profile.

26. (Previously Added) The system of claim 25, further comprising an analysis system to analyze *in situ* parameters provided by the detecting system.

27. (Previously Added) The system of claim 26, the analysis system additionally analyzes *in situ* parameters based on at least one from a group consisting of current *in situ* parameters, previous *in situ* parameters, scatterometry signature profiles, and predetermined multi-sloped profiles.

28. (Previously Added) The system of claim 25, further comprising a storage medium for storing at least one from a group consisting of current *in situ* parameters, previous *in situ* parameters, scatterometry signature profiles, and predetermined multi-sloped profiles.

29. (Previously Added) A system for manufacturing semiconductor devices, comprising:  
means for etching at least one device to conform to a desired multi-sloped profile;  
means for detecting *in situ* parameters of the etching of the device utilizing scatterometry; and  
means for adjusting the etching of the multi-sloped profile as necessary to produce the desired multi-sloped profile.

30. (Withdrawn)